IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

KIMURA et al — Atty. Ref.: 1035-471

Serial No. 10/670,194 — Group: 1632

Filed: September 26, 2003 — Examiner:

For: CHIP-STACK SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME

* * * * * * * * * * *

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Further to applicants' Supplemental Information Disclosure Statement of January 9, 2004, applicants herewith submit a further corrected Form PTO-1449 (i.e., the U.S. reference which was omitted on the PTO-1449 submitted January 9, 2004 has been added and the "ABSTR" has been moved into the "translation - yes" column for the two Japanese references).

Respectfully submitted,
NIXON & VANDERHYE P.C.

February 4, 2004

By: _____
H. Warren Burnam, Jr.
Reg. No. 29,366

HWB:lsh
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100

Sheet 1 of 1

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
1035-471	10/670,194
APPLICANT	
KIMURA et al	
FILING DATE	**GROUP**
September 26, 2003	1632

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,184,060	02/2001	SINIAGUINE			

FOREIGN PATENT DOCUMENTS

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		223833/1998	08/1998	JAPAN			ABSTR	
		3186941	05/2001	JAPAN			ABSTR	

OTHER DOCUMENTS (including Author, Title, Date, Pertinent pages, etc.)

*Examiner | Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.

Form PTO-FB-A820 (Also PTO-1449)